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*Admitted only in Maryland * Admitted only in Virginia •Practice Limited to Federal Agencies

April 20, 2004

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Art Unit 2811

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Re:

U.S. Utility Patent Application

Application No. 10/697,286; Filed: October 31, 2003

For: Memory Cell for Modification of Default Register Values in an

Integrated Circuit Chip

Inventors:

Catalasan et al.

Our Ref:

1875.4360004

Sir:

Transmitted herewith for appropriate action are the following documents:

- 1. Information Disclosure Statement;
- 2. Form PTO-1449 listing the cited documents (1 page);
- 3. Copies of the three (3) cited documents; and
- 4. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Commissioner for Patents April 20, 2004 Page 2

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Donald J. Featherstone Attorney for Applicants Registration No. 33,876

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

CATALASAN et al.

Appl. No.: 10/697,286

Filed: October 31, 2003

For: Memory Cell for Modification of Default Register Values in an Integrated Circuit Chip Confirmation No.: 8428

Art Unit: 2811

Examiner: To Be Assigned

Atty. Docket: 1875.4360004

Information Disclosure Statement

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent

application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this
 Information Disclosure Statement was cited in a communication from a foreign
 patent office in a counterpart application and this communication was not
 received by any individual designated in 37 C.F.R.
 § 1.56(c) more than thirty
 days prior to the filing of this information disclosure statement.
- 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.
 - a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

	□ b.	Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of
	,	information in this Information Disclosure Statement was cited in a
		communication from a foreign patent office in a counterpart foreign
		application and, to my knowledge after making reasonable inquiry, was
		known to any individual designated in 37 C.F.R. § 1.56(c) more than
		three months prior to the filing of this Information Disclosure Statement.
		37 C.F.R. § 1.97(e)(2).
	□ c.	Attached is our PTO-2038 Credit Card Payment Form in the amount of
		\$ in payment of the fee under 37 C.F.R. § 1.17(p).
4 .	Filing	under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being
	filed n	nore than three months after the U.S. filing date and after the mailing date
	of a Fi	nal Rejection or Notice of Allowance, but before payment of the Issue Fee.
	Enclos	sed find our PTO-2038 Credit Card Payment Form in the amount of
	\$	in payment of the fee under 37 C.F.R. § 1.17(p); in addition:
	□ a.	Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of
		information contained in this Information Disclosure Statement was cited
		in a communication from a foreign patent office in a counterpart foreign
		application not more than three months prior to the filing of this
		Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
	□ b.	Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of
		information in this Information Disclosure Statement was cited in a
		communication from a foreign patent office in a counterpart foreign

application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

<u></u> 5.	The document(s) was/were cited in a search report by a foreign patent office in a
	counterpart foreign application. Submission of an English language version of
	the search report that indicates the degree of relevance found by the foreign office
	is provided in satisfaction of the requirement for a concise explanation of
	relevance. 1138 OG 37, 38.
<u> </u>	A concise explanation of the relevance of the non-English language document(s) appears below:
⊠ 7.	Copies of documents AR1, AS1, and AT1 are submitted herewith.
8 .	Copies of the documents were cited by or submitted to the Office in an IDS that
	complies with 37 C.F.R. § 1.98(a)-(c) in Application No, filed
	, which is relied upon for an earlier filing date under 35 U.S.C.
	§ 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).
9 .	No copies of U.S. patents and patent application publications cited on the
	attached Form PTO-1449 are submitted in accordance with 1276 OG 55 because
	this application was filed after June 30, 2003.
<u> </u>	. It is expected that the examiner will review the prosecution and cited art in the

parent application no. _____ in accordance with MPEP 2001.06(b), and

indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Donald Y. Featherstone Attorney for Applicants Registration No. 33,876

Date: 4

1100 New York Avenue, N.W. Washington, D.C. 20005-3934 (202) 371-2600

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						ATTY. DOCKET NO. APPLICATION NO. 1875.4360004 10/697,286						
FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT							TORS					
							CATALASAN et al. FILING DATE October 31, 2003			ART UNIT		
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	AR	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Catalasan et al., U.S. Patent Appl. No. 10/697,079, filed October 31, 2003, entitled "Memory Cell For Modification Of Revision Identifier In An Integrated Circuit Chip," 54 pages.										
	AS	1 For Ma	Catalasan <i>et al.</i> , U.S. Patent Appl. No. 10/697,889, filed October 31, 2003, entitled "Method For Manufacturing A Memory Cell For Modification Of Revision Identifier In An Integrated Circuit Chip," 53 pages.									
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